AMENDMENTS TO THE DRAWINGS:

Please amend the drawings as follows:

On Sheet 1, in Figure 5C, add the reference --500c-- with an arrow pointing to the circuit.

On Sheet 3, in Figure 4:

add --ddb<1>--, --ddb<3>--,--ddb<4>--,--ddb<5>--,--ddb<6>-- and --ddb<7>-- referring to the inputs of the inverters having outputs "dd<1>", "dd<3>", "dd<4>", "dd<5>", "dd<6>" and "dd<7>", respectively;

change "dd<4>" to --ddb<4>-- and "dd<6>" to --ddb<6>-- at the input of the upper NAND gate 72 in dashed box 70;

change "dd<5>" to --ddb<5>-- and "dd<7>" to --ddb<7>-- at the input of the lower NAND gate 72 in dashed box 70;

change "dd<5>" to --ddb<5>-- at the input of the upper NAND gate 82 in dashed box 80;

change "dd<7>" to --ddb<7>-- and "dd<3>" to --ddb<3>-- at the input of the lower NAND gate 82 in dashed box 80;

change "dd<5>" to --ddb<5>-- and "dd<3>" to --ddb<3>-- at the input of the upper NAND gate 92 in dashed box 90;and

change "dd<7>" to --ddb<7>-- and "dd<1>" to --ddb<1>-- at the input of the lower NAND gate 92 in dashed box 90.

On Sheet 4, in Figure 5A, add the reference --500a-- with an arrow pointing to the circuit.

On Sheet 5, in Figure 5B, add the reference --500b-- with an arrow pointing to the circuit.

All of these changes are shown in red on accompanying correction Sheets 1 and 3-5, and are included in accompanying formal replacement Sheets 1 and 3-5.

REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1, 3, 4, 7, 12 and 13 are in the case. Claim 1 has been amended. The Specification has been amended. The Drawings have been amended.

Regarding the requirement of correction of the Brief Description of the Drawing, such correction has been made.

Regarding the requirement of inclusion of description of Figures 5A-5C, such description has been added herein. Figures 5A-5C have been amended to conform to this description.

Regarding the requirement for change of "adapted to" to --configured to--, this formal change has been made.

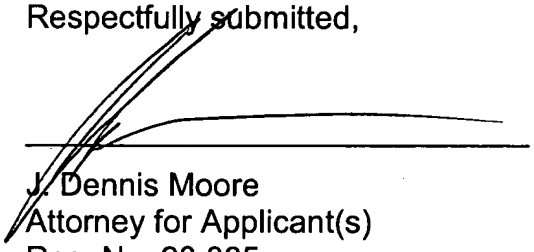
Numerous other changes of a formal nature have been made to improve form and to correct minor informalities throughout the Specification, in order to place the document in better form for issuance. For example, it was discovered that certain inverse logic levels of signals in Figure 4 were inadvertently omitted. However, the logic of the circuit only works when the appropriate level is provided to the respective NAND gate input, which can be worked out straightforwardly. No new matter has been added in any of the amendments made herein.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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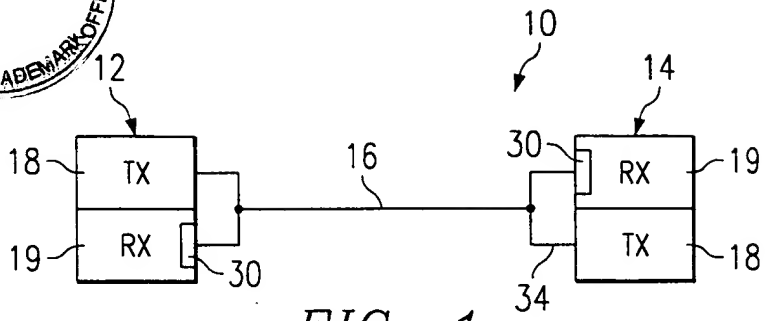

FIG. 1

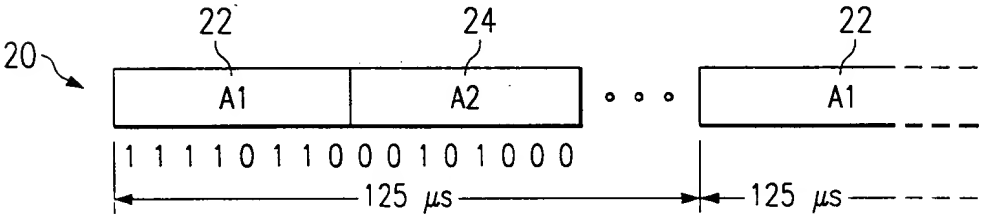

FIG. 2

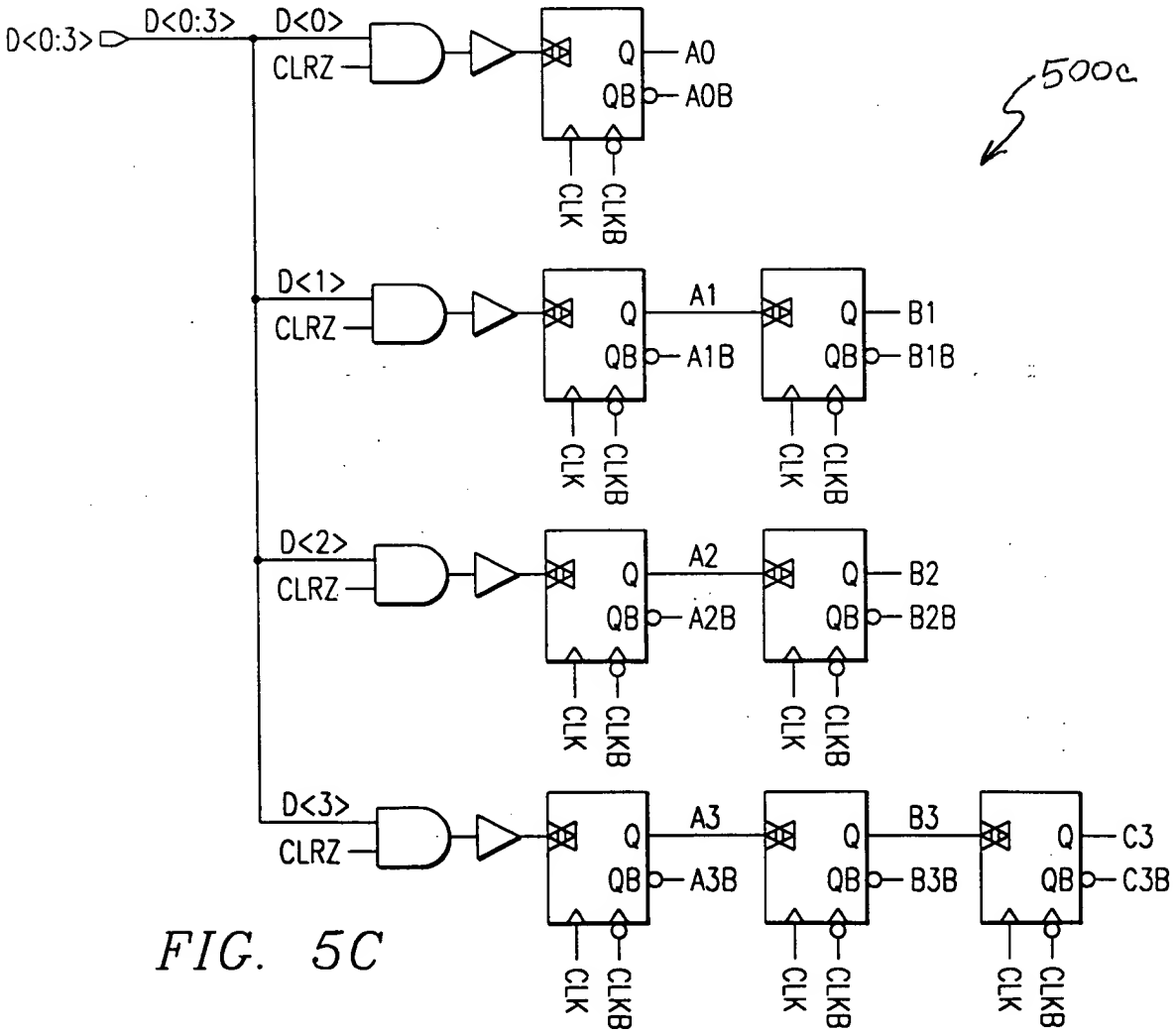

FIG. 5C

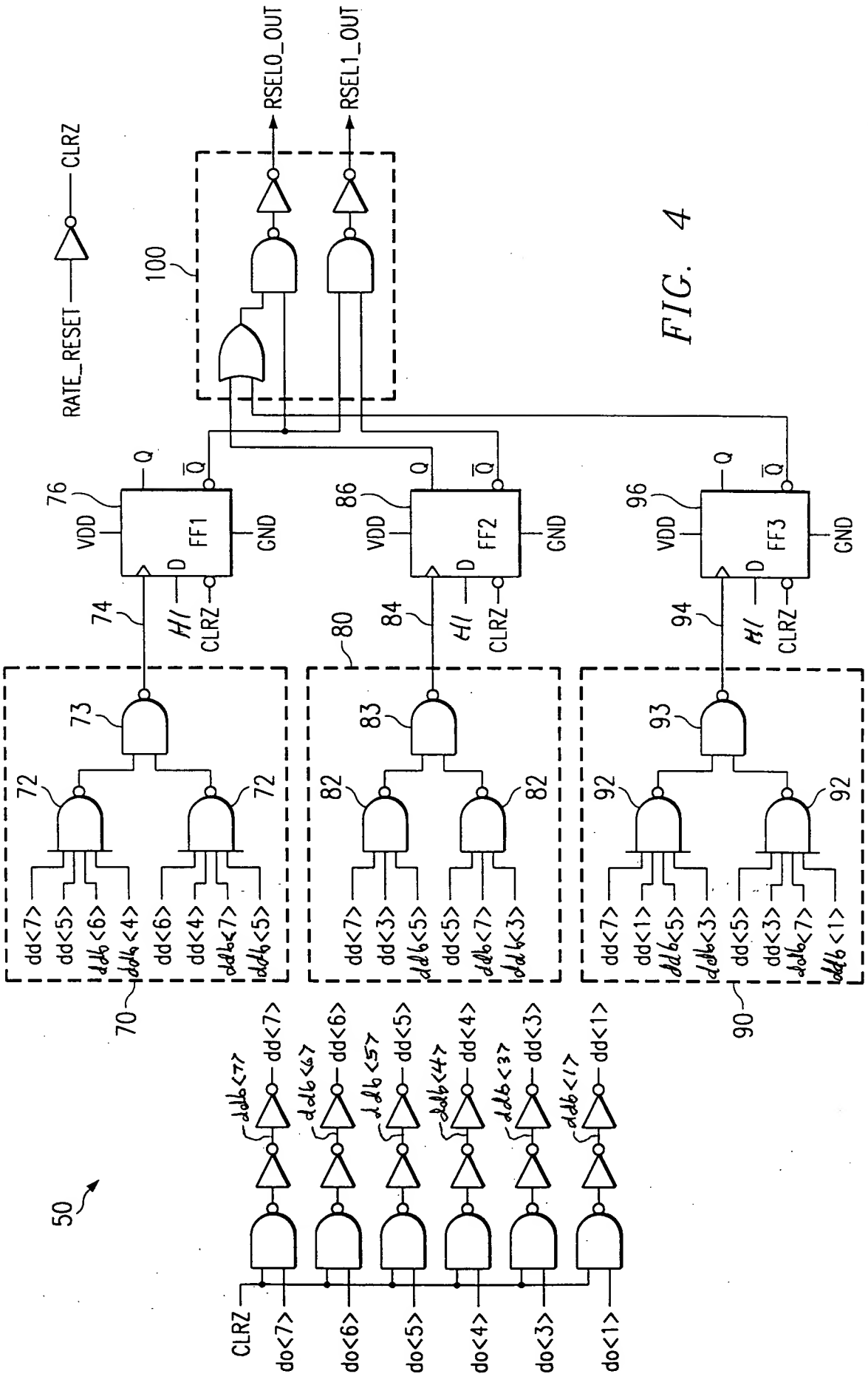
RSEL0_OUT
RSEL1_OUT
RATE_RESET
CLRZ
100
76
86
96
VDD
GND
FF1
FF2
FF3
D
Q
$\overline{Q}$
74
80
84
94
HI
CLRZ
73
83
93
72
82
92
dd<7>
dd<5>
ddb<6>
ddb<4>
dd<6>
dd<4>
ddb<7>
ddb<5>
dd<3>
ddb<3>
dd<1>
ddb<1>
70
90
50
ddb<7>
ddb<6>
ddb<5>
ddb<4>
ddb<3>
ddb<1>
do<7>
do<6>
do<5>
do<4>
do<3>
do<1>

FIG. 4

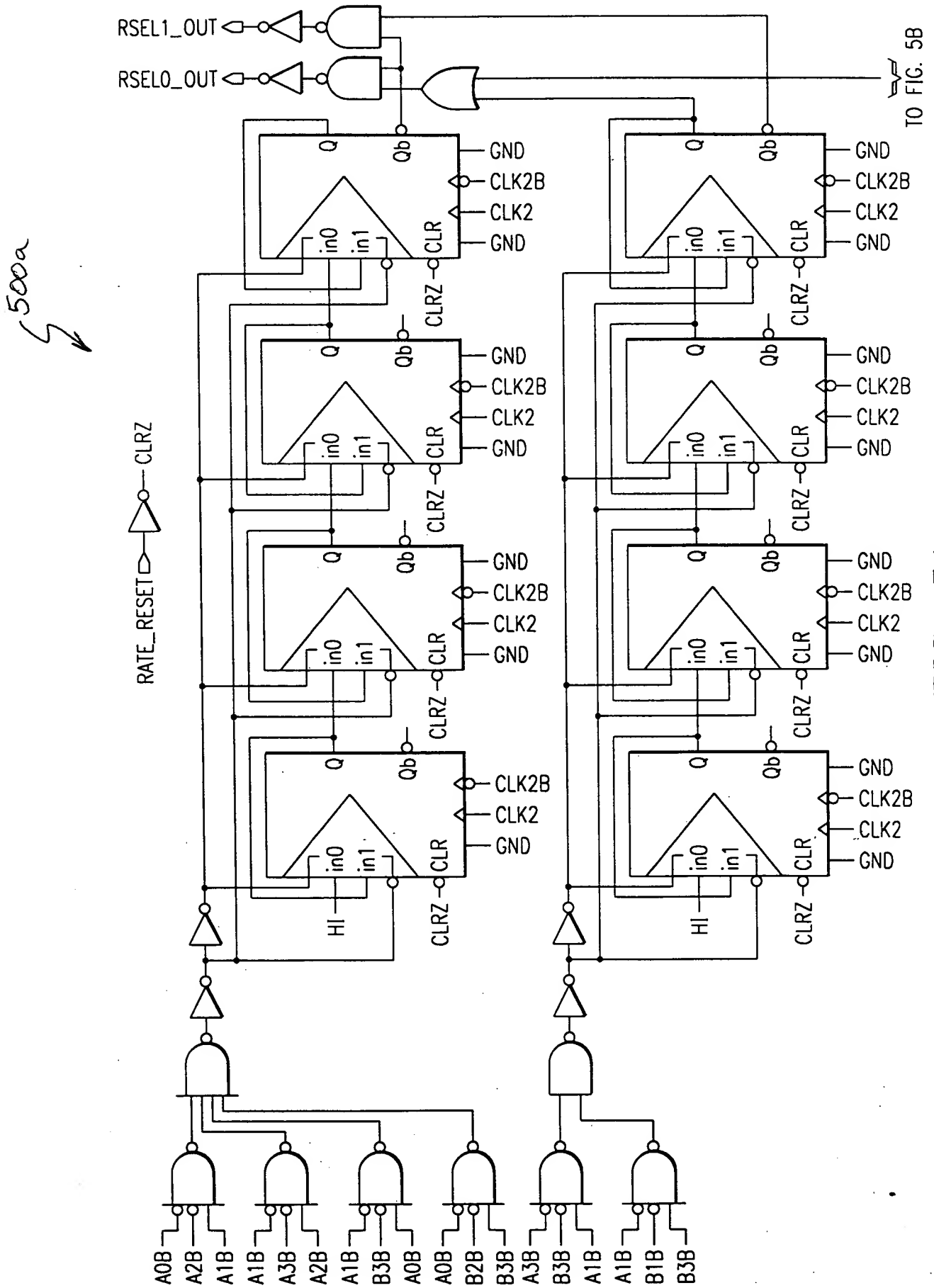
RSEL1_OUT
RSEL0_OUT
TO FIG. 5B
500a
RATE_RESET
CLRZ
Q
Qb
in0
in1
CLR
GND
CLK2B
CLK2
HI
A0B A2B A1B
A1B A3B A2B
A1B B3B A0B
A0B B2B B3B
A3B B3B A1B
A1B B1B B3B

FIG. 5A

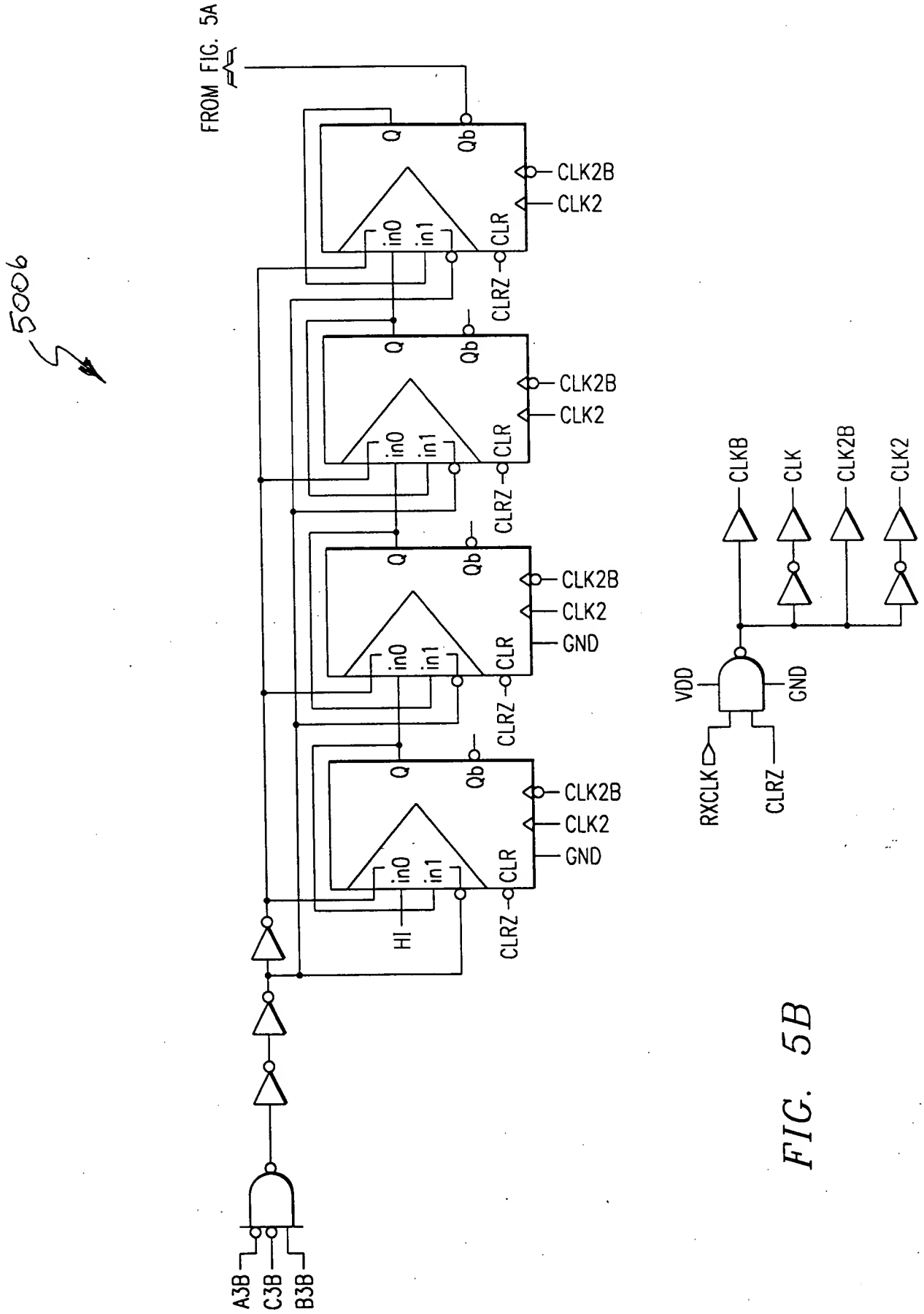
5006
FROM FIG. 5A
Q
Qb
CLK2B
CLK2
in0
in1
CLR
CLRZ
GND
HI
A3B
C3B
B3B
CLKB
CLK
VDD
RXCLK

FIG. 5B